In re Patent Application of
RAYNOR
Serial No. **10/786,878**
Filed: **FEBRUARY 25, 2004**

REMARKS

Applicants appreciate the Examiner's careful and thorough examination of the present application, and for correctly withdrawing the previous rejection. By this amendment, independent Claims 11 and 20 have been amended to further clarify the features of the present invention. Various dependent claims have been amended or canceled for consistency with the amendments to the independent claims. Also, new dependent Claim 36 has been added. Claims 11, 12, 14-21, 23-26 and 36 are pending in the application. Favorable reconsideration is respectfully requested.

I. The Claimed Invention

Independent Claim 1 is directed to an image sensing structure including a photodiode comprising a layer of a first conductivity type, and a well of a second conductivity type having opposing sides and positioned in the layer. The well defines a collection node. The photodiode further comprises an isolation trench at least partially bounding an upper portion of the well at the opposing sides thereof and comprising a shallow trench isolation (STI) having a depth from the upper surface of the layer less than the depth of the well. Independent Claim 20 is directed to a CMOS image sensing structure comprising a semiconductor substrate, and the photodiode of Claim 11 in the semiconductor substrate. In addition, the layer is of a P-type conductivity, and the well is of an N-type conductivity.

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II. The Claims are Patentable

Claims 11-26 were rejected in view of Rhodes (U.S. 6,723,594) for the reasons set forth on pages 2-4 of the Office Action. Applicant contends that Claims 11 and 20 clearly define over the cited reference, and in view of the following remarks, favorable reconsideration of the rejections under 35 U.S.C. §102 and §103 is requested.

As set forth above, each of the independent Claims 11 and 20 include the isolation trench at least partially bounding an upper portion of the well at the opposing sides thereof and comprising a shallow trench isolation (STI) having a depth from the upper surface of the layer less than the depth of the well. It is these combinations of features which are not fairly taught or suggested in the cited reference and which patentably define over the cited reference.

The Examiner has relied on the Rhodes '594 patent as disclosing a structure (FIG. 11) in which a well 30 is at least partly circumscribed by field oxide layers 112, which may be provided by a shallow trench isolation (STI) process.

Claims 11 and 20 have been amended to recite that the isolation trench comprises an STI, and that the trench has a depth less than the depth of the well. New claim 36 requires that the depth of the STI is about 2 mm and that the depth of the well is about 3 mm.

Rhodes '594 is directed CMOS image sensors having a high storage capacitance due to increased surface area of the gates of the source follower. In other words, the object of Rhodes '594 is increased gate size. The present invention, in contrast, seeks to improve the consistency of the capacitance

of the photodiode itself as between the various pixels of the array. This is achieved by better controlling the width of the photodiode wells. The invention is based upon use of trenching to give a well-defined and accurate edge to the well before implantation. Rhodes '594 forms the N-well 30 (Fig. 6) before the oxide isolation 112 (Fig. 7). Therefore, it is believed that the accuracy of the N-well width in Rhodes '594 will be no better than any other typical prior art N-well implantation process.

Moreover, the present invention provides a high level of quantum efficiency by providing a relatively deep N-well. The invention, as defined in amended claim 11, makes use of the fact that the desired level of accuracy can be achieved by using STI to define the area for implantation but with the N-well extending deeper into the silicon. This is discussed in the specification. New claim 36 attaches preferred dimensions to this. As discussed at page 6, paragraph No. [0024], a depth of 2 μm is conventional in transistor manufacture, and thus the structure of Claim 36 has the benefit of being readily producible by standard manufacturing techniques.

As the Examiner is aware, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim.

There is simply no teaching or suggestion in the cited reference to provide the combination of features as claimed. Accordingly, for at least the reasons given above, Applicant maintains that the cited reference does not disclose

or fairly suggest the invention as set forth in Claims 1 and 20. Furthermore, no proper modification of the teachings of this reference could result in the invention as claimed. Thus, the prior art rejections should be withdrawn.

It is submitted that the independent claims are patentable over the prior art. In view of the patentability of the independent claims, it is submitted that their dependent claims, which recite yet further distinguishing features are also patentable over the cited references for at least the reasons set forth above. Accordingly, these dependent claims require no further discussion herein.

III. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance. An early notice thereof is earnestly solicited. If, after reviewing this Response, there are any remaining informalities which need to be resolved before the application can be passed to issue, the Examiner is invited and respectfully requested to contact the undersigned by telephone in order to resolve such informalities.

Respectfully submitted,

PAUL J. DITMYER
Reg. No. 40,455
Allen, Dyer P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330
Attorney for Applicant